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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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Shannon E. Lawson

LAWSON 4

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11/24/2006

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EXAMINER

WARE, CICELY Q

ART UNIT

PAPER NUMBER

2611

DATE MAILED: 11/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/821,898

Applicant(s)

LAWSON, SHANNON E.

Examiner

Cicely Ware

Art Unit

2611

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 11 September 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)          | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____                                      |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)          | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____  | 6) <input type="checkbox"/> Other: _____                          |

## **DETAILED ACTION**

### ***Response to Arguments***

1. Applicant's arguments filed 9/11/2006 have been fully considered but they are not persuasive.

a. On Pg. 2-4 of applicant's **REMARKS/ARGUMENTS** applicant asserts that Nguyen does not disclose "generating an event signal based upon a first clock rate". Examiner disagrees. Examiner asserts that in fact Nguyen discloses data vectors (Fig. 1) as the signals, which are generated by element (62) in the first clock domain and transferred to a memory device in the second clock domain. Examiner asserts that these data vectors are the event signals. Therefore Nguyen does disclose "generating an event signal based upon a first clock rate". The rejection to claim 1 stands.

b. On Pg. 4-5 of applicant's **REMARKS/ARGUMENTS** applicant asserts that Radi does not teach "generating an event signal or synchronizing an event signal to a second clock rate based upon an edge transition of the event signal and the second clock rate". Examiner agrees with what Radi does not disclose. However Examiner asserts that Nguyen is used to disclose this element in claim 16. Radi is used for another element in the claim in which applicant did not address. Therefore the rejection to claim 16 stands.

### ***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

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A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claim 1, 6 and 11 are rejected under 35 U.S.C. 102(b) as being anticipated by Nguyen (US Patent 5,905,766).

(1) With regard to claim 1, Nguyen discloses in (Figs. 1 and 2) an event edge synchronization system (Fig. 2 (50)), comprising: a first clock zone device (Fig. 2 (20, 52)) configured to generate an event signal based upon a first clock rate; a second clock zone device (Fig. 2 (22, 58)) configured to operate at a second clock rate, which is asynchronous with said first clock rate (col. 1, lines 13-16); a synchronous notification subsystem (Fig. 2 (flip-flop #3)) configured to receive said event signal, synchronize said event signal to said second clock rate based upon an edge transition of said event signal and said second clock rate, and generate a synchronous notification signal therefrom.

(2) With regard to claim 6, see rejection of claim 1.

(3) With regard to claim 11, see rejection of claim 1.

### ***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 2-4, 5, 7-9, 10, 12-15 rejected under 35 U.S.C. 103(a) as being anticipated by Nguyen (US Patent 5,905,766) as applied to claim 1, in view of Cole et al. (US Patent 6,260,152).

(1) With regard to claim 2, claim 2 inherits all the limitations of claim 1. However Nguyen does not disclose synchronous notification subsystem includes: a first logic device configured to generate a first intermediate signal based upon said event signal and a clock signal of said second clock zone device; a second logic device configured to generate a second intermediate signal based upon said first intermediate signal and said clock signal of said second clock zone device; a third logic device configured to generate a third intermediate signal based upon said second intermediate signal and said clock signal of said second clock zone device; and a comparison logic device configured to generate said synchronous notification signal based upon said second and third intermediate signals.

However Cole et al. discloses in (Fig. 2) synchronous notification subsystem (30) includes: a first logic device (32) configured to generate a first intermediate signal based upon said event signal and a clock signal of said second clock zone device; a second logic device (34) configured to generate a second intermediate signal based upon said first intermediate signal and said clock signal of said second clock zone device; a third logic device (36) configured to generate a third intermediate signal based upon said second intermediate signal and said clock signal of said second clock zone device; and a comparison logic device (38) configured to generate said synchronous notification

signal based upon said second and third intermediate signals (abstract, col. 3, lines 3-21, col. 4, lines 1-18).

Therefore it would have been obvious to one of ordinary skill in the art to modify Nguyen to incorporate synchronous notification subsystem includes: a first logic device configured to generate a first intermediate signal based upon said event signal and a clock signal of said second clock zone device; a second logic device configured to generate a second intermediate signal based upon said first intermediate signal and said clock signal of said second clock zone device; a third logic device configured to generate a third intermediate signal based upon said second intermediate signal and said clock signal of said second clock zone device; and a comparison logic device configured to generate said synchronous notification signal based upon said second and third intermediate signals in order to improve synchronizing digital signals responsive to both positive and negative input edges, which result in lower power consumption, manufacturing costs, and failure rates (Cole et al, col. 2, lines 12-16).

(2) With regard to claim 3, claim 3 inherits all the limitations of claim 2. Cole et al. further discloses in (Fig. 2) wherein the first (32), second (34), and third (36) logic devices are "D" type flip-flops.

(3) With regard to claim 4, claim 4 inherits all the limitations of claim 2. Cole et al. further discloses in (Fig. 2) wherein the comparison logic device is an exclusive-OR (XOR) gate (38).

(4) With regard to claim 5, claim 5 inherits all the limitations of claim 1. Cole et al. further discloses in (Fig. 3) wherein said synchronous notification subsystem (Fig. 2

(30)) synchronizes said event signal (LSB) to said second clock rate (CLK2) based upon a positive edge transition of said event signal.

(5) With regard to claim 7, claim 7 inherits all the limitations of claim 6. See rejection of claim 2.

(6) With regard to claim 8, claim 8 inherits all the limitations of claim 7. See rejection of claim 3.

(7) With regard to claim 9, claim 9 inherits all the limitations of claim 7. See rejection of claim 4.

(8) With regard to claim 10, claim 10 inherits all the limitations of claim 6. See rejection of claim 5.

(9) With regard to claim 12, claim 12 inherits all the limitations of claim 11. See rejection of claim 2.

(10) With regard to claim 13, claim 13 inherits all the limitations of claim 12. See rejection of claim 3.

(11) With regard to claim 14, claim 14 inherits all the limitations of claim 12. See rejection of claim 4.

(12) With regard to claim 15, claim 15 inherits all the limitations of claim 11. See rejection of claim 5.

6. Claims 16-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nguyen (US Patent 5,905,766) in view of Cole et al. (US Patent 6,260,152) as applied to claim 1 in view of Radi (US Patent 6,594,327).

(1) With regard to claim 16, claim 16 inherits all the limitations of claim 1. Nguyen in combination with Cole et al. further discloses a first-in-first-out (FIFO) buffer (Nguyen, col. 1, lines 50-67).

However Nguyen in combination with Cole et al. do not disclose a fast pattern processor, comprising: a data buffer that stores processing blocks associated with a protocol data unit (PDU); a context memory subsystem associated with said data buffer that receives said processing blocks; a pattern processing engine, associated with said context memory, that performs pattern matching upon said processing blocks; and an output interface subsystem that receives said processing blocks from said data buffer or said context memory subsystem and re-transmits packets or payloads embodied within said processing blocks, said output interface subsystem.

However Radi discloses in (Figs. 1 and 2) a fast pattern processor (100), comprising: a data buffer (206) that stores processing blocks associated with a protocol data unit (PDU) (col. 4, lines 26-31); a context memory subsystem (206) associated with said data buffer that receives said processing blocks; a pattern processing engine (206), associated with said context memory, that performs pattern matching upon said processing blocks (col. 4, lines 3-15); and an output interface subsystem (Fig. 1 (106, 104)) that receives said processing blocks from said data buffer or said context memory subsystem and re-transmits packets or payloads embodied within said processing blocks, said output interface subsystem (col. 3, lines 3-6, 11-29, 35-43).

Therefore it would have been obvious to one of ordinary skill in the art to modify Nguyen in view of Radi to incorporate a fast pattern processor, comprising: a data buffer



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that stores processing blocks associated with a protocol data unit (PDU); a context memory subsystem associated with said data buffer that receives said processing blocks; a pattern processing engine, associated with said context memory, that performs pattern matching upon said processing blocks; and an output interface subsystem that receives said processing blocks from said data buffer or said context memory subsystem and re-transmits packets or payloads embodied within said processing blocks, said output interface subsystem in order to provide a synchronizer that can be used for two different standards or protocol (Radi, col. 2, lines 6-20).

(2) With regard to claim 17, claim 17 inherits all the limitations of claim 16. Cole et al. further discloses in (Fig. 2) synchronous notification subsystem (30) includes: a first logic device (32) configured to generate a first intermediate signal based upon said event signal and a clock signal of said second clock zone device; a second logic device (34) configured to generate a second intermediate signal based upon said first intermediate signal and said clock signal of said second clock zone device; a third logic device (36) configured to generate a third intermediate signal based upon said second intermediate signal and said clock signal of said second clock zone device; and a comparison logic device (38) configured to generate said synchronous notification signal based upon said second and third intermediate signals (abstract, col. 3, lines 3-21, col. 4, lines 1-18).

(3) With regard to claim 18, claim 3 inherits all the limitations of claim 17. Cole et al. further discloses in (Fig. 2) wherein the first (32), second (34), and third (36) logic devices are "D" type flip-flops.

(4) With regard to claim 19, claim 4 inherits all the limitations of claim 17. Cole et al. further discloses in (Fig. 2) wherein the comparison logic device is an exclusive-OR (XOR) gate (38).

(5) With regard to claim 20, claim 20 inherits all the limitations of claim 16. Cole et al. further discloses in (Fig. 3) wherein said synchronous notification subsystem (Fig. 2 (30)) synchronizes said event signal (LSB) to said second clock rate (CLK2) based upon a positive edge transition of said event signal.

### ***Conclusion***

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cicely Ware whose telephone number is 571-272-3047. The examiner can normally be reached on Monday – Friday, 8-5.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammed Ghayour can be reached on 571-272-3021. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9314 for regular communications and 703-872-9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

*Cicely Ware*

cqw  
November 20, 2006

*M. G.*  
MOHAMMED GHAYOUR  
SUPERVISORY PATENT EXAMINER